REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

A few minor changes have been made to the specification.

Claims 1-19 are present in this application. Under 35 U.S.C. § 102(b), claims 1 and 13 are rejected over U.S. 6,507,011 (Ang) and claim 3 is rejected over U.S. 2003/0193579 (Mori et al). Under 35 U.S.C. § 103(a), claims 2, 14 and 19 are rejected over Ang and claim 18 is rejected over U.S. 5,077,602 (Moberg) in view of Mori et al. Claims 7-12 and 17 are allowed and claims 4-6, 15 and 16 were indicated as being allowable if written in independent form.

The Applicant greatly appreciates the allowance of claims 7-12 and 17 and the indication of patentable subject matter in claims 4-6, 15 and 16. Claim 4 is rewritten into independent form, and is thus in condition for allowance.

Claim 1 recites an image processing apparatus having an input terminal, a plurality of defective pixel correction circuits and a defective pixel correction timing generator. The plurality of defective pixel correction circuits correct the plurality of color component signals in parallel at the same time with predetermining timing. The Applicant respectfully requests withdrawal of the rejection of claim 1 since Ang does not disclose all of the elements of claim 1, and thus cannot be used to reject claim 1 under 35 U.S.C. § 102(b).

Ang is directed to an active pixel color linear sensor. As shown in Figure 3, focal plane array 310 contains red, green and blue image sensor arrays 311-313. Line control/readout logic circuit 320 includes first, second and third readout register arrays 321-323 coupled to the arrays 311-313 by way of line store select logic 330. Figure 7 shows that the arrays are two-row linear arrays and readout register arrays 321-323 are also two-row configuration. The Office Action asserts that register arrays 321-323 are defective pixel correction circuits for correcting the plurality of the color component signals. However, there

is no description whatsoever in Ang of correcting any pixels. Register arrays 321-323 are designed to store the data from the arrays 311-313 without any corrective function. While the Office Action asserts that a corrective operation takes place, there is no reference to any description in Ang of such correction. The Applicant submits that no such disclosure exists. Thus, there is no plurality of defective pixel correction circuits and there is no defective pixel correction timing generator disclosed in Ang. There is further no disclosure of the defective pixel correction circuits correcting the plurality of color components in parallel at the same time with predetermined timing.

The rejection of claim 1 must be withdrawn since Ang does not disclose all of the elements of claim 1, and withdrawal thereof is respectfully requested. If this rejection is maintained, the Applicant respectfully requests specific identification of support for the assertion that Ang discloses defective pixel correction circuits.

Claim 3 recites an image processing apparatus having an input terminal for receiving a YUV signal. The YUV signal includes a luminance signal and a color difference signal. The apparatus also includes a selector for selecting one of the YUV signal and a plurality of color component signals, where the input terminal is shared by the YUV signal and the plurality of color component signals. A non-limiting example is illustrated in Figures 2 and 3 and described beginning on page 17. Color component signals R, G and B are input to terminals P2, P6 and P7, respectively. The YUV signal is 16 bits. The upper four bits are input to terminal P1 and the lower 12 bits are input to terminal P2. Input terminal P2 is shared by the YUV signals and the primary color component signals.

In Mori et al, as shown in Figure 3, YC separating circuit 3 receives the input video signal and video signals delayed by 1H and 2H. A luminance signal Yh, a vertical contour signal Vap, and R, G and B signals are outputted on separate terminals. The Yh and Yap signals are processed by the Y process circuit 4 and the RGB signals are processed by the

color difference matrix circuit 5. Separately inputted to the tone and hue correcting circuit 100 is the output of the Y process circuit 4 and two difference signals R-Y and B-Y. There is no input terminal which shares the YUV signal and one of the color component signals. Withdrawal of the §102 rejection based upon Mori et al of claim 3 is respectfully requested.

Claim 18 recites an image capture apparatus having a plurality of input terminals for receiving a YUV signal and a plurality of color component signals. One of the input terminals of the image processing apparatus is shared by the YUV signals and the plurality of color component signals. The Office Action relies upon Moberg to teach an apparatus receiving a YUV signal, but finds it not to teach the fifth through seventh paragraphs of claim 18. The Office Action again relies upon Mori. Referring to the discussion of Mori above, there is no input terminal in Mori et al shared by the YUV signal and one of the plurality of color component signals. As evident from the description of Mori et al above, the input terminals are separate and not shared. Accordingly, claim 18 is patentable over the combination of Moberg and Mori et al.

Claims 13 and 19 recite an image processing system and an image capture system, respectively, having a signal processor for processing a plurality of image signals in parallel, including phase adjustment in parallel and defective pixel correction in parallel, a plurality of output control circuits for outputting the plurality of image signals which are processed by said signal processor, to a bus, respectively, and a data transfer controller for transferring the plurality of image signals output to the bus. Ang does not disclose a processor which corrects defective pixels, and further does not disclose or suggest a processor which corrects defective pixels in parallel. Claims 13 and 19 are patentable over Ang.

Claim 15 is amended to include the elements of claim 13, without the elements of claim 14. It is respectfully submitted that claim 15 is patentably distinguishable over the cited prior art since none of these references discloses or suggests an image sensor which

functions to output two image signals read out in opposite directions, a plurality of output control circuits to output the two image signals, and a data transfer controller which functions to make an order or write addresses of one of the two image signals reversed relative to an order of write addresses of the other of the two image signals. Accordingly, allowance of claim 15 is respectfully requested.

It is respectfully submitted that the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

Respectfully submitted,

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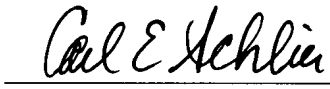

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